CLAIMS

What is claimed is:

1. A method of reconfiguring a complex programmable logic device (CPLD) in an electronic system, the CPLD comprising an electrically-erasable programmable read-only memory (EEPROM) array, a static random access memory (SRAM) array, a control circuit for loading data from the EEPROM array into the SRAM array and including a security circuit for protecting the data stored in the EEPROM array and the SRAM array, and a plurality of macrocells connected by a programmable interconnect matrix, the method comprising:

storing a first set of configuration data in the SRAM array to configure the plurality of macrocells and the programmable interconnect matrix to place the CPLD in a first configuration, the first set of configuration data comprising a security code used by the security circuit to prevent writing to the EEPROM array except under a set of limited circumstances; and

programming the EEPROM array with a second set of configuration data while operating the electronic system with the CPLD in the first configuration.

2. The method of Claim 1, wherein the set of limited circumstances includes the application of an erase pulse to the EEPROM array, the erase pulse being of at least a predetermined duration sufficient to ensure erasure of the first set of configuration data from the EEPROM array.

3. The method of Claim 2, wherein the erase pulse is of a longer duration than is required to ensure erasure of the first set of configuration data from the EEPROM array.

4. The method of Claim 1, wherein the set of limited circumstances includes the placement of the CPLD in a predetermined operational mode.

5. The method of Claim 1, further comprising loading the second set of configuration data from the EEPROM array into the SRAM array without terminating normal operation of the electronic system.

6. The method of Claim 5, wherein the second set of configuration data in the SRAM array places the CPLD in a second configuration, the method further comprising:

programming the EEPROM array with a third set of configuration data while operating the CPLD in the second configuration; and

loading the third set of configuration data from the EEPROM array into the SRAM array without terminating normal operation of the electronic system.

7. The method of Claim 1, further comprising:

removing power from the CPLD; and

restoring power to the CPLD, wherein the SRAM array reads the second set of configuration data from the EEPROM array when power is restored to the CPLD.

8. The method of Claim 7, further comprising:

programming the EEPROM array with a third set of configuration data while operating the electronic system with the CPLD in the second configuration; and

loading the third set of configuration data from the EEPROM array into the SRAM array without terminating normal operation of the electronic system.

9. A computer readable storage medium storing an instruction for a complex programmable logic device (CPLD), the CPLD comprising a first electrically-erasable programmable read-only memory (EEPROM) array, a static random access memory (SRAM) array, a control circuit configured to load data from the first EEPROM array into the SRAM array and including a security circuit for protecting the data stored in the EEPROM array and the SRAM array, and a plurality of macrocells connected by a programmable interconnect matrix, the medium comprising:

code for storing a first set of configuration data in the SRAM array to configure the plurality of macrocells and the programmable interconnect matrix to place the CPLD in a first configuration, the first set of configuration data comprising a security code used by the security circuit to prevent writing to the EEPROM array except under a set of limited circumstances; and

code for programming the EEPROM array with a second set of configuration data while operating the electronic system with the CPLD in the first configuration.

10. The computer readable storage medium of Claim 9, wherein the set of limited circumstances includes the application of an erase pulse to the EEPROM array, the erase pulse being of at least a predetermined duration sufficient to ensure erasure of the first set of configuration data from the EEPROM array.

11. The computer readable storage medium of Claim 10, wherein the erase pulse is of a longer duration than is required to ensure erasure of the first set of configuration data from the EEPROM array.

12. The computer readable storage medium of Claim 9, wherein the set of limited circumstances includes the placement of the CPLD in a predetermined operational mode.

13. The computer readable storage medium of Claim 9, wherein the computer-readable storage medium comprises a floppy disk.

14. The computer readable storage medium of Claim 9, wherein the computer-readable storage medium comprises a CDROM.

15. The computer readable storage medium of Claim 9, wherein the computer-readable storage medium comprises a hard drive accessible across a network.

16. A complex programmable logic device (CPLD) in an electronic system, the CPLD comprising:

an electrically-erasable programmable read-only memory (EEPROM) array;

a static random access memory (SRAM) array;

a control circuit for loading data from the EEPROM array into the SRAM array and including a security circuit for protecting the data stored in the EEPROM array and the SRAM array;

a programmable interconnect matrix;

a plurality of macrocells interconnected by the programmable interconnect matrix;

means for storing a first set of configuration data in the SRAM array to configure the plurality of macrocells and the programmable interconnect matrix to place the CPLD in a first configuration, the first set of configuration data comprising a security code used by the security circuit to prevent writing to the EEPROM array except under a set of limited circumstances; and

means for programming the EEPROM array with a second set of configuration data while operating the electronic system with the CPLD in the first configuration.

17. A complex programmable logic device (CPLD), comprising:

a configuration data input terminal;

an electrically-erasable programmable read-only memory (EEPROM) array;

a static random access memory (SRAM) array;

a control circuit coupled to the plurality of input terminals, the EEPROM array, and the SRAM array, wherein the control circuit is configured to load data from the configuration data input terminal to the EEPROM array and further configured to load data from the EEPROM array to the SRAM array;

a programmable interconnect matrix coupled to the SRAM array; and

a plurality of macrocells coupled to the SRAM array and interconnected by the programmable interconnect matrix, wherein the SRAM array configures the plurality of macrocells and the programmable interconnect matrix to configure the CPLD, wherein:

the EEPROM array comprises a first security location storing a first security code;

the SRAM array comprises a second security location storing a second security code; and

the control circuit comprises a security circuit coupled to the second security location, the security circuit preventing writing to the EEPROM array except under a set of limited circumstances.

18. The CPLD of Claim 17, wherein the EEPROM array is programmable without affecting normal operation of the CPLD.

19. The CPLD of Claim 17, wherein the security circuit comprises a first security output terminal and a security override output terminal, an active signal on the security override output terminal overriding an active signal on the first security output terminal.

20. The CPLD of Claim 19, wherein:

the CPLD further comprises an erase pulse input terminal coupled to erase data stored in the EEPROM array on receipt of an erase pulse; and

the security circuit comprises a timer circuit having an input terminal coupled to the erase pulse input terminal, the timer circuit being coupled to provide the active signal on the security override output terminal when the erase pulse reaches a predetermined length.

21. A method of reconfiguring a complex programmable logic device (CPLD) in an electronic system, the CPLD comprising an electrically-erasable programmable read-only memory (EEPROM) array, a static random access memory (SRAM) array, a control circuit for loading data from the EEPROM array into the SRAM array and including a security circuit for protecting the data stored in the EEPROM array and the SRAM array, and a plurality of macrocells connected by a programmable interconnect matrix, the method comprising:

programming the EEPROM array with a first set of configuration data;

transferring the first set of configuration data from the EEPROM array to the SRAM array under control of the control circuit, the first set of configuration data comprising a security code used by the security circuit to prevent writing to the EEPROM array except under a set of limited circumstances;

operating the CPLD in a first configuration based on the first set of configuration data transferred to the SRAM array;

erasing the EEPROM array after transferring the first set of configuration data from the EEPROM array to the SRAM array and while operating the electronic system with the CPLD in the first configuration; and

reprogramming the EEPROM array with a second set of configuration data while operating the electronic system with the CPLD in the first configuration.

22. The method of Claim 21, wherein the set of limited circumstances includes the application of an erase pulse to the EEPROM array, the erase pulse being of at least a predetermined duration sufficient to ensure erasure of the first set of configuration data from the EEPROM array.

23. The method of Claim 22, wherein the erase pulse is of a longer duration than is required to ensure erasure of the first set of configuration data from the EEPROM array.

24. The method of Claim 21, wherein the set of limited circumstances includes the placement of the CPLD in a predetermined operational mode.

25. The method of Claim 21, further comprising:

transferring the second set of configuration data from the EEPROM array to the SRAM array under control of the control circuit; and

operating the CPLD in a second configuration based on the second set of configuration data transferred to the SRAM array.

26. The method of Claim 25, wherein transferring the second set of configuration data from the EEPROM array to the SRAM array comprises transferring the second set of configuration data from the EEPROM array to the SRAM array without terminating normal operation of the electronic system.

27. The method of Claim 21, further comprising:

removing power from the CPLD; and

restoring power to the CPLD, wherein the SRAM array reads the second set of configuration data from the EEPROM array when power is restored to the CPLD.

28. A computer readable storage medium storing an instruction for a complex programmable logic device (CPLD), the CPLD comprising a first electrically-erasable programmable read-only memory (EEPROM) array, a static random access memory (SRAM) array, a control circuit configured to load data from the first EEPROM array into the SRAM array and including a security circuit for protecting the data stored in the EEPROM array and the SRAM array, and a plurality of macrocells connected by a programmable interconnect matrix, the medium comprising:

code for programming the EEPROM array with a first set of configuration data;

code for transferring the first set of configuration data from the EEPROM array to the SRAM array under control of the control circuit, the first set of configuration data comprising a security code used by the security circuit to prevent writing to the EEPROM array except under a set of limited circumstances;

code for operating the CPLD in a first configuration based on the first set of configuration data transferred to the SRAM array;

code for erasing the EEPROM array after transferring the first set of configuration data from the EEPROM array to the SRAM array and while operating the electronic system with the CPLD in the first configuration; and

code for reprogramming the EEPROM array with a second set of configuration data while operating the electronic system with the CPLD in the first configuration.

29. The computer readable storage medium of Claim 28, wherein the set of limited circumstances includes the application of an erase pulse to the EEPROM array, the erase pulse being of at least a predetermined duration sufficient to ensure erasure of the first set of configuration data from the EEPROM array.

30. The computer readable storage medium of Claim 29, wherein the erase pulse is of a longer duration than is required to ensure erasure of the first set of configuration data from the EEPROM array.

31. The computer readable storage medium of Claim 28, wherein the set of limited circumstances includes the placement of the CPLD in a predetermined operational mode.

32. The computer readable storage medium of Claim 28, further comprising:

code for transferring the second set of configuration data from the EEPROM array to the SRAM array under control of the control circuit; and

code for operating the CPLD in a second configuration based on the second set of configuration data transferred to the SRAM array.

33. The computer readable storage medium of Claim 32, wherein the code for transferring the second set of configuration data from the EEPROM array to the SRAM array comprises code for transferring the second set of configuration data from the EEPROM array to the SRAM array without terminating normal operation of the electronic system.

34. The computer readable storage medium of Claim 28, further comprising:

code for removing power from the CPLD; and

code for restoring power to the CPLD, wherein the SRAM array reads the second set of configuration data from the EEPROM array when power is restored to the CPLD.

35. The computer readable storage medium of Claim 28, wherein the computer-readable storage medium comprises a floppy disk.

36. The computer readable storage medium of Claim 28, wherein the computer-readable storage medium comprises a CDROM.

37. The computer readable storage medium of Claim 28, wherein the computer-readable storage medium comprises a hard drive accessible across a network.

38. A complex programmable logic device (CPLD) in an electronic system, the CPLD comprising:

an electrically-erasable programmable read-only memory (EEPROM) array;

a static random access memory (SRAM) array;

a control circuit for loading data from the EEPROM array into the SRAM array and including a security circuit for protecting the data stored in the EEPROM array and the SRAM array;

a programmable interconnect matrix;

a plurality of macrocells interconnected by the programmable interconnect matrix;

means for programming the EEPROM array with a first set of configuration data;

means for transferring the first set of configuration data from the EEPROM array to the SRAM array under control of the control circuit, the first set of configuration data

comprising a security code used by the security circuit to prevent writing to the EEPROM array except under a set of limited circumstances;

means for operating the CPLD in a first configuration based on the first set of configuration data transferred to the SRAM array;

means for erasing the EEPROM array after transferring the first set of configuration data from the EEPROM array to the SRAM array and while operating the electronic system with the CPLD in the first configuration; and

means for reprogramming the EEPROM array with a second set of configuration data while operating the electronic system with the CPLD in the first configuration.